I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on November 18, 2003. The applicant and/or attorney requests the date of deposit as the filing date. Depositor: Karen Cinq-Mars

(Signature & date) 11/18/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : November 18, 2003

Chidambarrao, Dureseti, et al.: Group Art Unit: To Be Assigned

Serial No. 10/605,135: Examiner: To Be Assigned

Filed: 9/10/03 : International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533

TITLE: METHOD AND STRUCTURE FOR IMPROVED MOSFET'S USING POLY / SILICIDE GATE HEIGHT CONTROL

INFORMATION DISCLOSURE STATEMENT
Under 37 C.F.R. 1.56

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the documents listed on the attached Form PTO-1449 to the attention of the examiner in charge of the above-identified application.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. They are merely cited as constituting related art of which the applicant is aware.

It is respectfully requested that these documents be considered by the examiner and formally made of record in this application.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,
Dureseti Chidambarrao, et al.

By 11-18-03
Joseph P. Abate
Registration No. 30,238
Telephone No. 845-894-4633

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. FIS9-2003-0184-US1	SERIAL NO. 10/605,135
	APPLICANT: Chidambarrao, Dureseti, et al.	
	FILING DATE: 9/10/03	GROUP: Unassigned

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
		US 6,228,694 B1	5/8/2001	Doyle et al.			
		US 6,406,973 B1	6/18/2002	Lee			
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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
FIS920030184US1	10/605,135
Applicant(s)	
Chidambarrao, Dureseti, et al.	
Filing Date	**Group Art Unit**
9/10/03	Unassigned

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*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

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EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		NMOS Drive Current Reduction Caused by Transistor-Layout and Trench Isolation Induced Stress Gregory Scott, et al. 1999 IEEE, 34.4.1-34.4.4, IEDM 99-827 Transconductance Enhancement in Deep Submicron Strained-Si n- MOSFETs Kern (Ken) Rim, et al. 1998 IEEE, 26.8.1-26.8.4, IEDM 98-707
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